Exhibit K – Part 2

'366 Patent Anticipated or Rendered Obvious by Figure 1 of the '366 Patent, SMP211 Datasheet ("SMP211"), and PS07 schematics ("PS07")

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1. A pulse width modulated switch comprising	The SMP211 device in Figure 1 of the '366 is a pulse width modulated switch
a first terminal;	Figure 3 of the SMP211 datasheet shows a MOSFET switch with a drain
a second terminal;	Figure 3 of the SMP211 datasheet shows a MOSFET switch with a source
a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	Figure 3 of the SMP211 datasheet shows a MOSFET switch with a gate terminal that controls the switch, driven by a gate driver with a drive signal.
an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;	Figure 3 of the SMP211 datasheet shows an oscillator with a maximum duty cycle signal, D_{MAX}, and waveforms illustrate on- and off-states.
a drive circuit that provides said drive signal according to said maximum duty cycle signal; and	Figure 3 of the SMP211 datasheet shows the D_{MAX} signal drives a 3-input NAND gate which then drives a gate driver. The resulting drive signal has a duty cycle that cannot be greater that the duty cycle of D_{MAX}.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.	Figure 1 specification of '366 shows and describes a soft start circuit consisting of capacitor **110**. At startup, the capacitor charges, allowing current to flow through the LED in the opto-coupler, and provide a signal via the feedback path to disable the drive signal for a portion of the DMAX duty cycle. As capacitor **110** gradually charges up, the drive signal's duty cycle grows accordingly until normal regulation operation.
2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.	It is inherent or would be obvious to combine all of the regulation circuitry with soft start circuitry into a single monolithic device, consistent with trends in the semiconductor industry.
8. The pulse width modulated switch of claim 1 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	Figure 1 of '366 shows a diode bridge rectifier with an AC input and DC output.
a power supply capacitor that receives said rectified signal;	Figure 1 of '366 shows a power supply capacitor across the rectified DC output of the diode bridge rectifier.

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a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and	Figure 1 of '366 shows a transformer with one winding connected to the drain terminal of SMP211 device and the rectified DC voltage.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	Figure 1 of '366 shows a second winding magnetically coupled to the first winding and connected to the output (which should be DC OUT). The transformer circuit enables energy to be transferred from the first winding to a load connect to the DC OUTPUT.
9. A regulation circuit comprising	
a first terminal;	Figure 3 of the SMP211 datasheet shows a MOSFET switch with a drain
a second terminal;	Figure 3 of the SMP211 datasheet shows a MOSFET switch with a source
a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	Figure 3 of the SMP211 datasheet shows a MOSFET switch with a gate terminal that controls the switch, driven by a gate driver with a drive signal.
a drive circuit that provides said drive signal for a maximum time period of a cycle; and	Figure 3 of the SMP211 datasheet shows the D_{MAX} signal drives a 3-input NAND gate which then drives a gate driver. The resulting drive signal has a duty cycle that cannot be greater that the duty cycle of D_{MAX}.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.	Figure 1 and specification of '366 show and describe a soft start circuit consisting of capacitor **110**. At startup, the capacitor charges, allowing current to flow through the LED in the opto-coupler, and provide a signal via the feedback path to disable the drive signal for a portion of the DMAX duty cycle. As capacitor 110 gradually charges up, the drive signal's duty cycle grows accordingly until normal regulation operation.
10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.	Figure 3 of the SMP211 datasheet shows an oscillator with a maximum duty cycle signal, D_{MAX}, and waveforms illustrate on- and off-states. This D_{MAX} signal connects to the NAND gate preceding the gate driver.
14. The regulation circuit of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies	Figure 1 and the specification of '366 teach a frequency variation circuit consisting of a resistor **140** connected to the rectified DC voltage and node **125** of the SMP211 device. Variations in

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according to a magnitude of said frequency variation signal.	current **135** (the frequency variation signal), due to ripple on the rectified voltage **15**, causes the oscillator frequency to vary. The bandgap circuit in the PS07 schematics shows that fluctuations of current **135** vary an internal bias voltage that sets a current within the oscillator. This varying bias voltage in turn sets the oscillation frequency.
16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.	It is inherent or would be obvious to combine all of the regulation circuitry with soft start circuitry into a single monolithic device, consistent with trends in the semiconductor industry.
18. The regulation circuit of claim 9 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	Figure 1 of '366 shows a diode bridge rectifier with an AC input and DC output.
a power supply capacitor that receives said rectified signal;	Figure 1 of '366 shows a power supply capacitor across the rectified DC output of the diode bridge rectifier.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and	Figure 1 of '366 shows a transformer with one winding connected to the drain terminal of SMP211 device and the rectified DC voltage.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	Figure 1 of '366 shows a second winding magnetically coupled to the first winding and connected to the output (which should be DC OUT). The transformer circuit enables energy to be transferred from the first winding to a load connect to the DC OUTPUT.

'366 Patent Anticipated or Rendered Obvious by Unitrode Application Note U-128 ("U-128") and Unitrode Datasheets UC3823 ("UC3823"); UC3823A,B/3825A,B ("UC3823A"); and UC3828 ("UC3828").

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1. A pulse width modulated switch comprising	U-128 discloses "enhancements incorporated in four new PWM control ICs, UC3823A, UC3823B, UC3825A and UC3825B." Figure 2 of UC-128 shows a switch.
a first terminal;	Figure 2 of U-128 shows a MOSFET switch with a drain terminal.
a second terminal;	Figure 2 of U-128 shows a MOSFET switch with the source terminal.
a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	The gate terminal of Figure 2 in U-128 is driven by the controller IC with a drive signal that controls current flow between the drain and source of the switch.
an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;	The UC3823 datasheet shows an oscillator that has an output that drives a 2-input NOR gate. This oscillator output signal is a maximum duty cycle signal with on- and off-states.
a drive circuit that provides said drive signal according to said maximum duty cycle signal; and	The UC3823 datasheet further shows the 2-input NOR gate, connected to the oscillator, drives a driver buffer with a drive signal, Out. The maximum duty cycle signal sets the maximum duty cycle of this drive signal.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.	Figure 15 and pp. 10-234—10-235 in U-128 show and describe the soft start circuit. The soft start voltage is created by integrating current onto a capacitor. The soft start voltage feeds into the error amplifier, which disables the drive signal for a portion of the maximum duty cycle possible, to limit the duty cycle of the drive signal at startup.
2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.	It is inherent or would be obvious to combine all of the regulation circuitry into a single monolithic device, consistent with consistent trends in the semiconductor industry.
8. The pulse width modulated switch of claim 1 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	It is inherent or would be obvious that the high DC voltage input in Figure 2 of U-128 is generated by a rectifier circuit.
a power supply capacitor that receives said rectified signal;	It is inherent or would be obvious that the high DC voltage input in Figure 2 of U-128 is

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	generated by a rectifier circuit with a power supply capacitor.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and	Figure 2 of U-128 shows one winding of a transformer connected the drain terminal of the MOSFET switch (driven by the PWM controller) and the high DC input voltage.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	Figure 2 of U-128 shows a second winding magnetically coupled to the first and connects to the OUTPUT. It is inherent or would be obvious that the OUTPUT connects to a load. This transformer circuit enables energy delivery from the first winding to the output (load).
9. A regulation circuit comprising	
a first terminal;	Figure 2 of U-128 shows a MOSFET switch with a drain terminal.
a second terminal;	Figure 2 of U-128 shows a MOSFET switch with the source terminal.
a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	The gate terminal of Figure 2 in U-128 is driven by the controller IC with a drive signal that controls current flow between the drain and source of the switch.
a drive circuit that provides said drive signal for a maximum time period of a cycle; and	The UC3823 datasheet further shows the 2-input NOR gate, connected to the oscillator, drives a driver buffer with a drive signal, Out. The maximum duty cycle signal from the oscillator sets the maximum duty cycle of this drive signal.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.	Figure 15 and pp. 10-234—10-235 in U-128 show and describe the soft start circuit. The soft start voltage is created by integrating current onto a capacitor. The soft start voltage feeds into the error amplifier, which disables the drive signal for a portion of the maximum duty cycle possible, to limit the duty cycle of the drive signal at startup.
10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.	The UC3823 datasheet shows an oscillator that has an output that drives a 2-input NOR gate. This oscillator output signal is a maximum duty cycle signal with on- and off-states.
14. The regulation circuit of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and	It is inherent or would have been obvious for the regulation circuit of claim 9 further comprising a frequency variation circuit that provides a

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wherein said maximum time period varies according to a magnitude of said frequency variation signal.	frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.
16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.	It is inherent or would be obvious to combine all of the regulation circuitry into a single monolithic device, consistent with consistent trends in the semiconductor industry.
18. The regulation circuit of claim 9 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	It is inherent or would be obvious that the high DC voltage input in Figure 2 of U-128 is generated by a rectifier circuit.
a power supply capacitor that receives said rectified signal;	It is inherent or would be obvious that the high DC voltage input in Figure 2 of U-128 is generated by a rectifier circuit with a power supply capacitor.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and	Figure 2 of U-128 shows one winding of a transformer connected the drain terminal of the MOSFET switch (driven by the PWM controller) and the high DC input voltage.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	Figure 2 of U-128 shows a second winding magnetically coupled to the first and connects to the OUTPUT. It is inherent or would be obvious that the OUTPUT connects to a load. This transformer circuit enables energy delivery from the first winding to the output (load).

'366 Patent Anticipated or Rendered Obvious by SGS-Thomson Application Note AN376 ("AN376") and datasheets for related devices TEA2260/61 ("TEA2260")

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1. A pulse width modulated switch comprising	TEA2260/61 datasheet pp. 2 and 3: The TEA2260 is a switch mode power supply controller using a PWM generator. Two embodiments of the TEA2260 anticipate the claims of the '366 patent.
a first terminal;	In the first embodiment: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 switch has a first terminal, V+, shown as pin 15. In the second embodiment: TEA2260/61 datasheet p. 2, Figure 2: The first terminal is the terminal of the external transistor connected to one terminal of the primary winding of the transformer.
a second terminal;	In the first embodiment: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 switch has a second terminal, OUT, shown as pin 14. In the second embodiment: TEA2260/61 datasheet p. 2, Figure 2: The second terminal is the terminal of the external transistor connected to ground through a sense resistor.
a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	In the first embodiment: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 switch includes a switch, i.e., a gate drive transistor switch, which has a control input (from a positive output stage). The gate drive transistor switch allows a signal to be transmitted between the first terminal, V+, and the second terminal, OUT, according to a drive signal provided at the control input from the positive output stage. In the second embodiment: TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 is connected to a switch comprising a control input, the switch allowing a signal to be transmitted between the first terminal and the second terminal according to a drive signal provided at said control input.

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an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;	In both embodiments: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 switch includes an oscillator, which provides a maximum duty cycle signal, i.e., a pulse signal, comprising an on-state and an off-state. AN376 p. 12, Figure 14: "An auxiliary PWM generates a maximum duty cycle conduction signal (β), by comparing the sawtooth with an internal fixed voltage." The sawtooth is generated by the oscillator.
a drive circuit that provides said drive signal according to said maximum duty cycle signal; and	In both embodiments: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 includes a drive circuit, which provides the drive signal according to the maximum duty cycle signal. AN376 p. 12 and 13, Figure 15: "A logic 'AND' between signals (α) and (β) provides the primary regulator output signal T_A." T_A feeds the drive circuit that creates the drive signal.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.	In both embodiments: AN376 p. 12, Figure 14: The TEA2260 includes a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal during at least a portion of the on-state of the maximum duty cycle. "during the starting phase of the SMPS, in association with an external capacitor, this PWM generates increasing duty cycle, thus allowing a 'soft' start-up."
2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.	In the first embodiment: TEA2260/61 datasheet p. 3, Block Diagram: The pulse width modulated switch, i.e., TEA2260 switch, is a monolithic integrated circuit, which contains the first terminal, second terminal, switch, oscillator, drive circuit, and soft start circuit.
8. The pulse width modulated switch of claim 1 further comprising	In the second embodiment: The TEA2260 meets every element of claim 1, as set forth above.

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a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 discloses a rectifier comprising an input and an output with the input receiving an AC mains signal and the output providing a rectified signal.
a power supply capacitor that receives said rectified signal;	TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 discloses a power supply capacitor that receives the rectified signal from the rectifier and provides a substantially DC signal.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and	TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 discloses a first winding having a first terminal and a second terminal. The first winding receives the substantially DC signal with the second terminal of the first winding coupled to the first terminal of the pulse modulated switch.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 discloses a second winding magnetically coupled to the first winding wherein the first winding is capable of being coupled to a load.
9. A regulation circuit comprising	TEA2260/61 datasheet pp. 2 and 3: The TEA2260 is a switch mode power supply controller. Two embodiments of the TEA2260 anticipate the claims of the '366 patent.
a first terminal;	In the first embodiment: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 switch has a first terminal, V+, shown as pin 15. In the second embodiment: TEA2260/61 datasheet p. 2, Figure 2: The first terminal is the terminal of the external transistor connected to one terminal of the primary winding of the transformer.
a second terminal;	In the first embodiment: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 switch has a second terminal, OUT, shown as pin 14. In the second embodiment: TEA2260/61 datasheet p. 2, Figure 2: The second terminal is the terminal of the external transistor connected to ground through a sense resistor.

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a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	In the first embodiment: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 switch includes a switch, i.e., a gate drive transistor switch, which has a control input (from a positive output stage). The gate drive transistor switch allows a signal to be transmitted between the first terminal, V+, and the second terminal, OUT, according to a drive signal provided at the control input from the positive output stage. In the second embodiment: TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 is connected to a switch comprising a control input, the switch allowing a signal to be transmitted between the first terminal and the second terminal according to a drive signal provided at said control input.
a drive circuit that provides said drive signal for a maximum time period of a cycle; and	In both embodiments: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 includes a drive circuit, which provides the drive signal according to the maximum duty cycle signal. AN376 p. 12 and 13, Figure 15: "A logic 'AND' between signals (α) and (β) provides the primary regulator output signal T_A." T_A feeds the drive circuit that creates the drive signal.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.	In both embodiments: AN376 p. 12, Figure 14: The TEA2260 includes a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal during at least a portion of the on-state of the maximum duty cycle. "during the starting phase of the SMPS, in association with an external capacitor, this PWM generates increasing duty cycle, thus allowing a 'soft' start-up."
10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.	In both embodiments: TEA2260/61 datasheet p. 3, Block Diagram: The TEA2260 switch includes an oscillator, which provides a maximum duty cycle signal, i.e., a pulse signal, comprising an on-state and an off-state.

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	AN376 p. 12, Figure 14: "An auxiliary PWM generates a maximum duty cycle conduction signal (β), by comparing the sawtooth with an internal fixed voltage." The sawtooth is generated by the oscillator.
14. The regulation circuit of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.	In both embodiments: AN376 (p. 32) Figure 44 teaches a frequency variation circuit consisting of a npn transistor that sinks current from pin 11, along with RC drive circuit to its base terminal. The operation is described on p. 32.
16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.	In the first embodiment: TEA2260/61 datasheet p. 3, Block Diagram: The pulse width modulated switch, i.e., TEA2260 switch, is a monolithic integrated circuit, which contains the first terminal, second terminal, switch, oscillator, drive circuit, and soft start circuit.
18. The regulation circuit of claim 9 further comprising	In the second embodiment: The TEA2260 meets every element of claim 1, as set forth above.
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 discloses a rectifier comprising an input and an output with the input receiving an AC mains signal and the output providing a rectified signal.
a power supply capacitor that receives said rectified signal;	TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 discloses a power supply capacitor that receives the rectified signal from the rectifier and provides a substantially DC signal.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and	TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 discloses a first winding having a first terminal and a second terminal. The first winding receives the substantially DC signal with the second terminal of the first winding coupled to the first terminal of the pulse modulated switch.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	TEA2260/61 datasheet p. 2, Figure 2: The TEA2260 discloses a second winding magnetically coupled to the first winding wherein the first winding is capable of being coupled to a load.

'366 Patent Anticipated or Rendered Obvious by "Off-Line PWM Switching Regulator IC Handles 3W" by Frank Goodenough, *Electronic Design*, March 22, 1990 (pp. 35-39), PWR-SMP3 datasheet, and PS03 schematics, which all correspond to the PWR-SMP3 device

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1. A pulse width modulated switch comprising	Power Integrations' PWR-SMP3 is a pulse width modulated switch.
a first terminal;	Figure 2 of the Goodenough article, Figure 3 of the datasheet, and Sheet 1 (PS03_top) of the schematics all show a drain terminal that corresponds to the first terminal
a second terminal;	Figure 2 of the Goodenough article, Figure 3 of the datasheet, and Sheet 1 (PS03_top) of the schematics all show a common ground terminal that corresponds to the second terminal
a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	Figure 2 of the Goodenough article, Figure 3 of the datasheet, and Sheet 1 (PS03_top) of the schematics all show a control (or gate) terminal of the switch that is driven by a driver with a drive signal
an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;	Figure 3 of the datasheet and Sheet 1 (PS03_top) of the schematics show an oscillator that provides an output with a maximum duty cycle signal, denoted as D_{MAX} and T, respectively
a drive circuit that provides said drive signal according to said maximum duty cycle signal; and	Figure 2 of the Goodenough article and Figure 3 of the datasheet show a drive circuit consisting of a NAND and inverter buffer (together implementing an AND function) that provides a drive signal. The maximum duty cycle signal is an input to the AND logic, which limits the drive signal to turn on the switch only when the maximum duty cycle signal is "high." As shown in Figure 2 of the Goodenough article, the PWR-SMP3 has a drive circuit that provides the drive signal according to the maximum duty cycle signal. The article states, "The basic PWM circuit is conventional. The 0-to-50% duty-cycle pulses from the oscillator turns on the FET switch through the NAND-gate and the FET-gate driver. The sawtooth (ramp) output of the oscillator runs to the PWM comparator which receives its other input from the output of the error amplifier (the output is a function of the difference between the supply's output voltage through the feedback path and the output of the 1/25-V bandgap reference). When the level of the ramp reaches the output of the error amplifier, the comparator flips and turns off the FET switch through the OR gate, PWM latch, NAND gate and driver." p. 36.

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	Sheet 1 (PS03_top) and Sheet 12 (smp1a_out_logic) of the schematics provide much more detail in regards to the drive circuit and resulting drive signal. These schematics also show that the drive signal is can only be "high" during the portion of a cycle when the maximum duty cycle signal is "high."
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.	The Goodenough article describes the soft start circuit corresponding to the PWR-SMP3 device. It states, "The soft-start circuit consists of a current source and an internal capacitor connected to an intermediate stage of the error amplifier. Until the capacitor is fully charged, the error amplifier output voltage is clamped low, limiting the duty cycle and peak current of the switch during startup." p. 38. The PS03 schematics also show this soft start circuit, which provides a signal instructing the drive circuit to disable during a portion of the maximum duty cycle signal. Sheet 1 (PS03_top) of the schematics show a SFT_STR node connected to a port of the err_amp block and to a capacitor. Sheet 14 (smp1a_err_amp) shows a switch (MN6) that shorts the SFT_STR node to ground when K is high. The K signal is generated by the fault_prot_logic block (Sheet 6, smp1a_fault_prot_logic), which starts "high" during startup (or under fault conditions) and transitions low. In the err_amp block, after K transitions from "high" to "low," current from MP10 charges up the SFT_STR node and the voltage on this node ramps up. When the voltage on the gate terminal of MP11 considerably less than the reference voltage on node VIN+, most of the current from MP11A flows through MP11, causing VOUT to be drive low. This occurs even if the parallel differential amplifier consisting of devices MP4, MP5, and MP2 is driven by an input condition that would try to force VOUT high. As the voltage on node SFT_STR rises, the voltage on VOUT also rises. It is important to note here that the ratio of currents between MP11A and MP2 enables the soft circuit to override the error amplification path. Moreover, the relatively narrow widths of MP11 and MP12 show that the amplifier connected to node SFT_STR was purposely made to have a wider operating input voltage range to enable the output VOUT to gradually follow the voltage ramp on node

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	SFT_STR. The voltage ramp on VOUT feeds into the fcomp block (Sheet 11, smp1a_fcomp), which compares the VOUT voltage to a SAWTOOTH signal from the oscillator. The output of the fcomp block sets the duty cycle of the drive signal. So, the soft start circuit described here limits the duty cycle of the drive signal. Moreover, the ascending voltage ramp on node SFT_STR causes the duty cycle to initially start out small and then increase. The limitation imposed on the duty cycle via the soft start circuitry occurs during the "high" portion of the maximum duty cycle signal.
2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.	Figure 2 of the article, Figure 3 of the datasheet, and Sheet 1 (PS03_top) of the schematics all show that all blocks listed in this claim are implemented within a single monolithic device.
8. The pulse width modulated switch of claim 1 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	As shown in Figure 2 of the Goodenough article, the PWM-SMP3 can be used with a rectifier (Bridge rectifier D_1) with a rectifier input and a rectifier output, the rectifier input receiving an AC mains signal and the rectifier output providing a rectifier signal. "To construct a complete switching regulator, all that's required are a bridge rectifier and filter, a storage inductor/isolation transformer, a Schottky diode, several other rectifiers and diodes, and a handful of resistors and capacitors, in addition to the PWR-SMP3 (*Fig. 2*)." p. 36. Figure 1 of the PWR-SMP3 datasheet shows a diode bridge rectifier with input AC IN and a rectified output.
a power supply capacitor that receives said rectified signal;	As shown in Figure 2 of the Goodenough article, the PWM-SMP3 can be used with a power supply capacitor (C_1) that receives the rectified signal. Figure 1 of the PWR-SMP3 datasheet shows a capacitor shunting the output of the diode bridge rectifier.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and	As shown in Figure 2 of the Goodenough article, the PWM-SMP3 can be used with a first winding comprising a first terminal and a second terminal, the first winding receiving a substantially DC signal from the power supply capacitor, the second terminal of the first winding coupled to the first terminal of the pulse width modulated switch.

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	Figure 1 of the PWR-SMP3 datasheet shows a transformer with a first winding that has one terminal connected to the DC output of the rectifier and the other terminal connected to the DRAIN terminal of the PWR-SMP3 device.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	As shown in Figure 2 of the Goodenough article, the PWM-SMP3 can be used with a second winding magnetically coupled to the first winding, the first winding capable of being coupled to a load. Figure 1 of the PWR-SMP3 datasheet shows a transformer with a second winding that is magnetically coupled to the first winding, consistent with the way a transformer operates. Moreover, this configuration provides a mechanism for providing energy to the load from the first winding.
9. A regulation circuit comprising	Power Integrations' PWR-SMP3 is a regulation circuit
a first terminal;	Figure 2 of the article, Figure 3 of the datasheet, and Sheet 1 (PS03_top) of the schematics all show a drain terminal that corresponds to the first terminal
a second terminal;	Figure 2 of the article, Figure 3 of the datasheet, and Sheet 1 (PS03_top) of the schematics all show a common ground terminal that corresponds to the second terminal
a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	Figure 2 of the Goodenough article, Figure 3 of the datasheet, and Sheet 1 (PS03_top) of the schematics all show a control (or gate) terminal of the switch that is driven by a driver with a drive signal
a drive circuit that provides said drive signal for a maximum time period of a cycle; and	As shown in Figure 2 of the Goodenough article, the PWR-SMP3 has a drive circuit that provides the drive signal for a maximum time period of a cycle. The article states, "The basic PWM circuit is conventional... The sawtooth (ramp) output of the oscillator runs to the PWM comparator which receives its other input from the output of the error amplifier (the output is a function of the difference between the supply's output voltage through the feedback path and the output of the 1/25-V bandgap reference). When the level of the ramp reaches the output of the error amplifier, the comparator flips and turns off the FET switch through the OR gate, PWM latch, NAND gate and driver." p. 36.

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	Figure 3 of the datasheet shows a drive circuit consisting of a NAND and inverter buffer (together implementing an AND function) that provides a drive signal. In this case, the maximum period of a cycle happens to be limited by the maximum duty cycle signal from the oscillator.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.	The same explanation used above for sixth element of Claim 1 can be used here. The maximum time period is understood to be the maximum time defined by the maximum duty cycle signal.
10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.	As shown in Figure 2 of the Goodenough article, the PWR-SMP3 has an oscillator that provides a maximum duty cycle signal to the drive circuit, the maximum duty cycle signal comprising an on-state for the maximum time period. Figure 3 of the PWR-SMP3 datasheet shows an oscillator that provides a maximum duty cycle signal, denoted as D_{MAX}, to the drive circuit comprising a NAND gate and inverter buffer.
14. The regulation circuit of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.	It is inherent or would be obvious for the regulation circuit to further comprise a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.
16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.	Figure 2 of the article, Figure 3 of the datasheet, and Sheet 1 (PS03_top) of the schematics all show that all blocks of the regulation circuits listed in this claim are implemented within a single monolithic device. The description section of the PWR-SMP3 datasheet states, "The PWR-SMP3, intended for off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit... The controller section of the PWR-SMP3 contains all the blocks required to drive and control the power stage: off-line start-up pre-regulator circuit, oscillator, bandgap reference voltage, error amplifier, gate driver, undervoltage lockout, over-temperature protection, and current limiting." p. 1-1.
18. The regulation circuit of claim 9 further comprising	
a rectifier input and a rectifier output, said	As shown in Figure 2 of the Goodenough article,

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rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	the PWM-SMP3 can be used with a rectifier (Bridge rectifier D_1) with a rectifier input and a rectifier output, the rectifier input receiving an AC mains signal and the rectifier output providing a rectifier signal. "To construct a complete switching regulator, all that's required are a bridge rectifier and filter, a storage inductor/isolation transformer, a Schottky diode, several other rectifiers and diodes, and a handful of resistors and capacitors, in addition to the PWR-SMP3 (*Fig. 2*)." p. 36. Figure 1 of the PWR-SMP3 datasheet shows a diode bridge rectifier with input AC IN and a rectified output.
a power supply capacitor that receives said rectified signal;	As shown in Figure 2 of the Goodenough article, the PWM-SMP3 can be used with a power supply capacitor (C_1) that receives the rectified signal. Figure 1 of the PWR-SMP3 datasheet shows a capacitor shunting the output of the diode bridge rectifier.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and	As shown in Figure 2 of the Goodenough article, the PWM-SMP3 can be used with a first winding comprising a first terminal and a second terminal, the first winding receiving a substantially DC signal from the power supply capacitor, the second terminal of the first winding coupled to the first terminal of the pulse width modulated switch. Figure 1 of the PWR-SMP3 datasheet shows a transformer with a first winding that has one terminal connected to the DC output of the rectifier and the other terminal connected to the DRAIN terminal of the PWR-SMP3 device.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	As shown in Figure 2 of the Goodenough article, the PWM-SMP3 can be used with a second winding magnetically coupled to the first winding, the first winding capable of being coupled to a load. Figure 1 of the PWR-SMP3 datasheet shows a transformer with a second winding that is magnetically coupled to the first winding, consistent with the way a transformer operates. Moreover, this configuration provides a mechanism for providing energy to the load from the first winding.

'366 Patent Anticipated or Rendered Obvious by "A 5A 100 KHz Monolithic Bipolar DC/DC Converter," by de Stasi and Szepesi, *The European Power Electronics Association*, 1993 (pp. 201-208) ("Stasi") and the related National Semiconductor LM1577/LM2577 ("LM2577") and LM2588 ("LM2588") datasheets

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1. A pulse width modulated switch comprising	Stasi discloses a pulse width modulated switch.
a first terminal;	As shown in Figure 1 of Stasi, there is a first terminal, Switch. "The new IC is a seven pin switching regulator with an open collector output switch. Fig. 1 shows the block diagram." Stasi, p. 201. Figure 4 in the LM2577 datasheet also shows a NPN switch with a collector terminal.
a second terminal;	As shown in Figure 1 of Stasi, there is a first terminal, Ground. "The new IC is a seven pin switching regulator with an open collector output switch. Fig. 1 shows the block diagram." Stasi, p. 201. Figure 4 in the LM2577 datasheet also shows a NPN switch with a emitter terminal.
a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	As shown in Figure 1 of Stasi, there is a switch comprising a control input, the switch allowing a signal to be transmitted between the first terminal and the second terminal according to a drive signal provided at the control input. "The new IC is a seven pin switching regulator with an open collector output switch. Fig. 1 shows the block diagram. The NPN power transistor can stand-off 70V and pass 5A peak currents" Stasi, p. 201. Figure 4 in the LM2577 datasheet has a base terminal connected to the driver stage providing a drive signal. The drive signal controls current through the switch.
an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;	As shown in Figure 1 of Stasi, there is an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state. "The trimmed 100 KHz oscillator requires no external components." Stasi, p. 201. Figure 4 in the LM2577 datasheet shows an oscillator connected to the logic block preceding the driver stage. Explanation on p. 3-91 says, "The LM1577/LM2577 turns its output switch on and off at a frequency of 52KHz..." The 52KHz frequency is generated by the oscillator.
a drive circuit that provides said drive signal	As shown in Figure 1 of Stasi, there is a drive

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according to said maximum duty cycle signal; and	circuit that provides the drive signal according to the maximum duty cycle signal. Figure 4 in the LM2577 datasheet also shows a driver stage.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.	As shown in Figures 1, 4, and 5a of Stasi, there is a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal during at least a portion of the on-state of the maximum duty cycle. "A soft- start feature can take over control of the loop and gradually increase the duty cycle from some small value to it's [sic] operating value." Stasi, p. 202. Figure 4 in the LM2577 datasheet shows a soft start circuit connected to the output of the error amplifier, which "reduces in-rush current during start-up." P. 3-80.
2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.	As shown in Figure 1 of Stasi, the first terminal, second terminal, switch, oscillator, drive circuit and soft start circuit comprise a monolithic device. "This paper describes a new monolithic boost/flyback switching regulator that is designed for ease of use in general purpose applications." Stasi, p. 201. "The soft-start feature of our new regulator is unique in that it does not require any additional external components." Stasi, p. 202.
8. The pulse width modulated switch of claim 1 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	It is inherent or would be obvious that the described pulse width modulated switch could be used in a flyback application circuit, which would include a rectifier input and a rectifier output, the rectifier input receiving an AC mains signal and the rectifier output providing a rectifier signal. "This paper describes a new monolithic boost/flyback switching regulator that is designed for ease of use in general purpose applications." Stasi, p. 201. Figure 15 in the LM2577 datasheet teaches the LM2577 used in a flyback regulator circuit.
a power supply capacitor that receives said rectified signal;	As shown in Figures 2 and 3 of Stasi, there is a power supply capacitor that receives the rectified signal.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first	As shown in Figures 2 and 3 of Stasi, there is a first winding comprising a first terminal and a second terminal, the first winding receiving a substantially DC signal from the power supply capacitor, the second terminal of the first winding

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terminal of said pulse width modulated switch; and	coupled to the first terminal of the pulse width modulated switch. Figure 15 in the LM2577 datasheet teaches the LM2577 used in a flyback regulator circuit. The switch terminal of the device (pin 4)is connected one terminal of the primary winding of a transformer. The other terminal is connected to a DC voltage, V_{IN}.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	It is inherent or would be obvious that the described pulse width modulated switch could be used in a flyback application circuit, which would include a second winding magnetically coupled to the first winding, the first winding capable of being coupled to a load. "This paper describes a new monolithic boost/flyback switching regulator that is designed for ease of use in general purpose applications." Stasi, p. 201. Figure 15 in the LM2577 datasheet teaches the LM2577 used in a flyback regulator circuit. The secondary winding connects to VOUT, which would drive a load. This flyback configuration allows energy form the primary winding to be delivered to the output (load).
9. A regulation circuit comprising	Stasi discloses a regulation circuit. "This paper describes a new monolithic boost/flyback switching regulator that is designed for ease of use in general purpose applications." Stasi, p. 201. LM2577 datasheet discloses a regulation circuit as presented in the General Description section, p. 3-80.
a first terminal;	As shown in Figure 1 of Stasi, there is a first terminal, Switch. "The new IC is a seven pin switching regulator with an open collector output switch. Fig. 1 shows the block diagram." Stasi, p. 201. Figure 4 in the LM2577 datasheet also shows a NPN switch with a collector terminal.
a second terminal;	As shown in Figure 1 of Stasi, there is a first terminal, Ground. "The new IC is a seven pin switching regulator with an open collector output switch. Fig. 1 shows the block diagram." Stasi, p. 201. Figure 4 in the LM2577 datasheet also shows a NPN switch with a emitter terminal.
a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second	As shown in Figure 1 of Stasi, there is a switch comprising a control input, the switch allowing a signal to be transmitted between the first terminal

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terminal according to a drive signal provided at said control input;	and the second terminal according to a drive signal provided at the control input. "The new IC is a seven pin switching regulator with an open collector output switch. Fig. 1 shows the block diagram. The NPN power transistor can stand-off 70V and pass 5A peak currents " Stasi, p. 201. Figure 4 in the LM2577 datasheet has a base terminal connected to the driver stage providing a drive signal. The drive signal controls current through the switch.
a drive circuit that provides said drive signal for a maximum time period of a cycle; and	As shown in Figure 1 of Stasi, there is a drive circuit that provides the drive signal for a maximum time period of a cycle. Figure 4 in the LM2577 datasheet also shows a driver stage.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.	As shown in Figures 1, 4, and 5a of Stasi, there is a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal during at least a portion of the maximum time period. "A soft- start feature can take over control of the loop and gradually increase the duty cycle from some small value to it's [sic] operating value." Stasi, p. 202. Figure 4 in the LM2577 datasheet shows a soft start circuit connected to the output of the error amplifier, which "reduces in-rush current during start-up." P. 3-80.
10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.	As shown in Figure 1 of Stasi, there is an oscillator that provides a maximum duty cycle signal to the drive circuit, the maximum duty cycle signal comprising an on-state for the maximum time period. "The trimmed 100 Khz oscillator requires no external components." Stasi, p. 201. Figure 4 in the LM2577 datasheet shows an oscillator connected to the logic block preceding the driver stage. Explanation on p. 3-91 says, "The LM1577/LM2577 turns its output switch on and off at a frequency of 52KHz..." The 52KHz frequency is generated by the oscillator.
14. The regulation circuit of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.	Stasi describes a frequency variation circuit that provides a frequency variation signal and wherein the maximum time period varies according to a magnitude of the frequency variation signal. "The on/off pin of the IC has a dual role; it can be used to shutdown the chip or to adjust the switching frequency. Pulling the on/off control high, puts the part in a shutdown mode where it draws only

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	50μA from the input supply. With the on/off control low, the part functions normally. If it is desired to increase the switching frequency, a resistor is connected from the on/off pin of the IC to ground." Stasi, p. 201. "To aid this situation, we simply reduce the switching frequency whenever the short-circuit condition is sensed.... As a result, the converter will operate in current limit at a much reduced switching frequency whenever the otput is shorted...." Stasi, p. 202. "In this regulator we monitor the voltage on the feedback pin, to detect the short-circuit condition. If this voltage drops below 0.6v (from the nominal 1.23v) the switching frequency is dropped to about 20 khz." Stasi, p. 202.
16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.	As shown in Figure 1 of Stasi, the first terminal, second terminal, switch, oscillator, drive circuit and soft start circuit comprise a monolithic device. "This paper describes a new monolithic boost/flyback switching regulator that is designed for ease of use in general purpose applications." Stasi, p. 201. "The soft-start feature of our new regulator is unique in that it does not require any additional external components." Stasi, p. 202.
18. The regulation circuit of claim 9 further comprising	As shown in Figure 1, there is a current limit circuit that provides a signal instructing the drive circuit to discontinue the drive signal when a current received at the first terminal of the regulation circuit is above a threshold level. "Several protective features are also included on the chip. They cycle-by-cycle current limit is set to keep the peak switch current below 6A." Stasi, p. 201. Figure 15 in the LM2577 datasheet teaches the LM2577 used in a flyback regulator circuit.
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	It is inherent or would be obvious that the described pulse width modulated switch could be used in a flyback application circuit, which would include a rectifier input and a rectifier output, the rectifier input receiving an AC mains signal and the rectifier output providing a rectifier signal. "This paper describes a new monolithic boost/flyback switching regulator that is designed for ease of use in general purpose applications." Stasi, p. 201. Figure 15 in the LM2577 datasheet teaches the LM2577 used in a flyback regulator circuit.
a power supply capacitor that receives said	As shown in Figures 2 and 3, there is a power

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rectified signal;	supply capacitor that receives the rectified signal.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and	As shown in Figures 2 and 3, there is a first winding comprising a first terminal and a second terminal, the first winding receiving a substantially DC signal from the power supply capacitor, the second terminal of the first winding coupled to the first terminal of the pulse width modulated switch. Figure 15 in the LM2577 datasheet teaches the LM2577 used in a flyback regulator circuit. The switch terminal of the device (pin 4)is connected one terminal of the primary winding of a transformer. The other terminal is connected to a DC voltage, V_{IN}.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	It is inherent or would be obvious that the described pulse width modulated switch could be used in a flyback application circuit, which would include a second winding magnetically coupled to the first winding, the first winding capable of being coupled to a load. "This paper describes a new monolithic boost/flyback switching regulator that is designed for ease of use in general purpose applications." Stasi, p. 201. Figure 15 in the LM2577 datasheet teaches the LM2577 used in a flyback regulator circuit. The secondary winding connects to VOUT, which would drive a load. This flyback configuration allows energy form the primary winding to be delivered to the output (load).

'366 Patent Anticipated or Rendered Obvious by National Semiconductor Application Note AN-918 ("AN-918"), Related Datasheets of LM3001 ("LM3001") and LM3101 ("LM3101") and US Patent No. 5,498,995 ("Szepesi")

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1. A pulse width modulated switch comprising	AN-918 describes a 1MHz off-line PWM controller chipset (LM3001/LM3101).
a first terminal;	Figure 8 of AN-918 shows a switch with a drain terminal connected to one terminal of a transformer.
a second terminal;	Figure 8 of AN-918 shows a switch with a source terminal connected to ground via a small sense resistor.
a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	The switch has a gate terminal that controls current flow between the drain and source terminals, and is driven by the output drive signal, V_{OUT}, of the LM3001 primary driver. Hence, the drive signal controls the switch.
an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;	The Block Diagram of the LM3001 datasheet shows an oscillator. Figure 2 shows a connection between the oscillator and the PWM comparator. The DUTY CYCLE LIMIT section describes how the maximum duty cycle signal is created within the PWM comparator. The Block Diagram of the LM3101 datasheet shows an oscillator that has an output that drives into a 3-input NOR gate and the S input of a SR flip-flop. This oscillator output signal acts as a maximum duty cycle signal with an on-state (logic "low") and an off-state (logic "high").
a drive circuit that provides said drive signal according to said maximum duty cycle signal; and	In the LM3001, the maximum duty cycle signal generated within PWM comparator limits the maximum duty cycle of the drive signal. In the LM3101, the above mentioned 3-input NOR gate feeds the OUTPUT DRIVER to provide a drive signal. Given the active-low nature of the maximum duty cycle, the NOR gate disables the switch during the off-state via the drive signal.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.	In the LM3001 data sheet, p. 3-148 describes the soft-start function. "The Soft-Start function limits the duty cycle at start-up." Figure 4 presents a soft-start timing diagram showing the drive signal's pulse width gradually increasing with respect to the soft-start voltage up to, but less than the duty cycle limit. In the LM3101 data sheet, p. 3-170 describes soft-

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	start, where "soft-start is accomplished by gradually increasing the reference voltage during start-up. The gradual increase is implemented by charging the soft-start capacitor…"
2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.	It is inherent or would be obvious to combine all of the regulation circuitry into a single monolithic device, consistent with consistent trends in the semiconductor industry.
8. The pulse width modulated switch of claim 1 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	Figure 8 of AN-918 illustrates an off-line voltage mode flyback regulator. The description in p. 5 explains, "The figure does no show the input diode bridge and EMI filter for simplicity..."
a power supply capacitor that receives said rectified signal;	Figure 8 of AN-918 illustrates an off-line voltage mode flyback regulator. The description in p. 5 explains, "The figure does no show the input diode bridge and EMI filter for simplicity..."
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and	Figure 8 of AN-918 shows one side of a transformer connected to the switch and the DC input voltage V_{IN}.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	Figure 8 of AN-918 a magnetically-coupled second winding that connects to the load. This circuit enables energy delivery from the first winding to the load.
9. A regulation circuit comprising	AN-918 describes a regulation circuit.
a first terminal;	Figure 8 of AN-918 shows a switch with a drain terminal connected to one terminal of a transformer.
a second terminal;	Figure 8 of AN-918 shows a switch with a source terminal connected to ground via a small sense resistor.
a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	The switch has a gate terminal that controls current flow between the drain and source terminals, and is driven by the output drive signal, V_{OUT}, of the LM3001 primary driver. Hence, the drive signal controls the switch.
a drive circuit that provides said drive signal for a maximum time period of a cycle; and	In the LM3001, the maximum duty cycle signal generated within PWM comparator limits the maximum duty cycle of the drive signal.

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	In the LM3101, the above mentioned 3-input NOR gate feeds the OUTPUT DRIVER to provide a drive signal. Given the active-low nature of the maximum duty cycle, the NOR gate disables the switch during the off-state via the drive signal.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.	In the LM3001 data sheet, p. 3-148 describes the soft-start function. "The Soft-Start function limits the duty cycle at start-up." Figure 4 presents a soft-start timing diagram showing the drive signal's pulse width gradually increasing with respect to the soft-start voltage up to, but less than the duty cycle limit. In the LM3101 data sheet, p. 3-170 describes soft-start, where "soft-start is accomplished by gradually increasing the reference voltage during start-up. The gradual increase is implemented by charging the soft-start capacitor…"
10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.	The Block Diagram of the LM3001 datasheet shows an oscillator. Figure 2 shows a connection between the oscillator and the PWM comparator. The DUTY CYCLE LIMIT section describes how the maximum duty cycle signal is created within the PWM comparator. The Block Diagram of the LM3101 datasheet shows an oscillator that has an output that drives into a 3-input NOR gate and the S input of a SR flip-flop. This oscillator output signal acts as a maximum duty cycle signal with an on-state (logic "low") and an off-state (logic "high").
14. The regulation circuit of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.	Figure 2 and p. 3-168 of the LM3101 datasheet show and describe a frequency variation circuit. "The LM3101 has the ability to gradually reduce its operating frequency during an output short circuit." The emitter voltage of Q2 in Figure 2 provides a frequency variation signal.
16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.	It is inherent or would be obvious to combine all of the regulation circuitry into a single monolithic device, consistent with consistent trends in the semiconductor industry.
18. The regulation circuit of claim 9 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	Figure 8 of AN-918 illustrates an off-line voltage mode flyback regulator. The description in p. 5 explains, "The figure does no show the input diode bridge and EMI filter for simplicity..."
a power supply capacitor that receives said	Figure 8 of AN-918 illustrates an off-line voltage

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rectified signal;	mode flyback regulator. The description in p. 5 explains, "The figure does no show the input diode bridge and EMI filter for simplicity..."
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and	Figure 8 of AN-918 shows one side of a transformer connected to the switch and the DC input voltage V_{IN}.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	Figure 8 of AN-918 a magnetically-coupled second winding that connects to the load. This circuit enables energy delivery from the first winding to the load.

'366 Patent Anticipated or Rendered Obvious by "Off-Line Power Integrated Circuit for International Rated 60-watt Power Supplies" by Richard Keller, Applied Power Electronics conference and Exposition, February 1992 (pp. 505-512) ("Keller") and SMP240/260 Datasheets

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1. A pulse width modulated switch comprising	
a first terminal;	As shown in Figures 1 and 11, Keller teaches a first terminal, Drain.
a second terminal;	As shown in Figures 1 and 11, Keller teaches a second terminal, Source.
a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	As shown in Figure 1, Keller teaches a switch comprising a control input, the switch allowing a signal to be transmitted between the first terminal (Drain) and the second terminal (Source) according to a drive signal provided at said control input.
an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;	As shown in Figure 1, Keller teaches an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state. *See* p. 508 ("The maximum duty cycle is user programmable."); *see also*, p. 509.
a drive circuit that provides said drive signal according to said maximum duty cycle signal; and	As shown in Figure 1, Keller teaches a drive circuit that provides the drive signal according to the maximum duty cycle signal.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.	As shown in Figure 1, Keller teaches a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal during at least a portion of the on-state of the maximum duty cycle. "During power up the circuit has an optional soft start function." P. 510. "When soft start is enabled the maximum output switch current is programmed linearly increasing from zero to maximum in 4096 power supply equivalent clock cycles." P. 510.
2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.	As shown in Figures 1 and 11, Keller teaches that the first terminal, second terminal, switch, oscillator, drive circuit and soft start circuit comprise a monolithic device.
8. The pulse width modulated switch of claim 1 further comprising	
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	As shown in Figure 11, Keller teaches a rectifier (BR1) input and a rectifier output, the rectifier input receiving an AC mains signal and the rectifier output providing a rectifier signal.

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a power supply capacitor that receives said rectified signal;	As shown in Figure 11, Keller teaches a power supply capacitor (C4 and/or C5) that receives said rectified signal.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and	As shown in Figure 11, Keller teaches a first winding comprising a first terminal and a second terminal, the winding receiving a substantially DC signal from the power supply capacitor, the second terminal of said first winding coupled to the first terminal of said pulse width modulated switch.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	As shown in Figure 11, Keller teaches a first winding comprising a first terminal and a second terminal, the first winding receiving a substantially DC signal from the power supply capacitor, the second terminal of the first winding coupled to the first terminal of the pulse width modulated switch.
9. A regulation circuit comprising	
a first terminal;	As shown in Figures 1 and 11, Keller teaches a first terminal, Drain.
a second terminal;	As shown in Figures 1 and 11, Keller teaches a second terminal, Source.
a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	As shown in Figure 1, Keller teaches a switch comprising a control input, the switch allowing a signal to be transmitted between the first terminal (Drain) and the second terminal (Source) according to a drive signal provided at said control input.
a drive circuit that provides said drive signal for a maximum time period of a cycle; and	As shown in Figure 1, Keller teaches a drive circuit that provides the drive signal for a maximum time period of a cycle.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.	As shown in Figure 1, Keller teaches a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal during at least a portion of the on-state of the maximum duty cycle. "During power up the circuit has an optional soft start function." P. 510. "When soft start is enabled the maximum output switch current is programmed linearly increasing from zero to maximum in 4096 power supply equivalent clock cycles." P. 510.
10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.	As shown in Figure 1, Keller teaches an oscillator that provides a maximum duty cycle signal to the drive circuit, the maximum duty cycle signal comprising an on-state for the maximum time period. *See* p. 508 ("The maximum duty cycle is user programmable."); *see also*, p. 509.

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14. The regulation circuit of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.	As shown in Figure 1, Keller teaches a frequency variation circuit that provides a frequency variation signal and wherein the maximum time period varies according to a magnitude of the frequency variation signal. "The oscillator frequency is set with a timing capacitor." P. 509. *See also* p. 508. Alternatively, a frequency variation circuit that provides a frequency variation signal and wherein the maximum time period varies according to a magnitude of the frequency variation signal would have been obvious to one of ordinary skill in the art in light of Keller.
16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.	As shown in Figures 1 and 11, Keller teaches that the first terminal, second terminal, switch, oscillator, drive circuit and soft start circuit comprise a monolithic device.
18. The regulation circuit of claim 9 further comprising	As shown in Figures 1 and 2, Keller teaches a current limit circuit that provides a signal instructing the drive circuit to discontinue the drive signal when a current received at the first terminal of the regulation circuit is above a threshold level. *See also*, p. 510 ("Protection features include input under voltage lockout, over temperature fault, output under voltage fault and output over current protection consistent with cycle by cycle peak limiting of the switch current.").
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	As shown in Figure 11, Keller teaches a rectifier (BR1) input and a rectifier output, the rectifier input receiving an AC mains signal and the rectifier output providing a rectifier signal.
a power supply capacitor that receives said rectified signal;	As shown in Figure 11, Keller teaches a power supply capacitor (C4 and/or C5) that receives said rectified signal.
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and	As shown in Figure 11, Keller teaches a first winding comprising a first terminal and a second terminal, the winding receiving a substantially DC signal from the power supply capacitor, the second terminal of said first winding coupled to the first terminal of said pulse width modulated switch.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	As shown in Figure 11, Keller teaches a first winding comprising a first terminal and a second terminal, the first winding receiving a substantially DC signal from the power supply capacitor, the second terminal of the first winding coupled to the first terminal of the pulse width

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	modulated switch.

'366 Patent Anticipated or Rendered Obvious by Unitrode App Note U-133 (UCC3800-series)

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1. A pulse width modulated switch comprising	Fig 1 shows a PWM controller IC, used with an outboard MOSFET switch as in Fig 28, 29, 30, 31, and 32. It is used without external switch in Fig 27.
a first terminal;	The MOSFETs have a drain terminal.
a second terminal;	The MOSFETs have a source terminal.
a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	The MOSFETs have a gate terminal that controls conduction from drain to source.
an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;	The oscillator has a maximum duty cycle, described at 9-348 and 9-349, whose signal is created by the flip-flop toggled by the sawtooth waveform tripping thresholds at 2.65V and 0.2V. For the UCC3801, -04, and -05 types there is a maximum duty cycle signal generated by the type-T flip-flop shown in Fig 1, and further described in the corresponding datasheets.
a drive circuit that provides said drive signal according to said maximum duty cycle signal; and	The drive circuit is shown in Fig 1, and consists at least of the SR flip-flop, gate, and output switch.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.	The soft-start circuit is shown in block diagram form in Fig 1, and described in greater detail at 9-352.
2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.	Fig 27 shows the UCC3803 in a buck converter with monolithic switch, oscillator, drive circuit, and soft-start circuit.
8. The pulse width modulated switch of claim 1 further comprising	
a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	Off-line applications are described at 9-358, understood by one of skill to be transformerless rectified and filtered AC line input. Explicit circuitry to that effect is shown in Unitrode App Notes U-96A and U-100A, both referenced in U-133.
a power supply capacitor that receives said rectified signal;	See above.
a first winding comprising a first terminal and a second terminal, said first winding	This configuration is shown in Fig 31.

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receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and	
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	Shown in Fig 31.
9. A regulation circuit comprising	Fig 1 shows a PWM controller IC, used with an outboard MOSFET switch as in Fig 28, 29, 30, 31, and 32. It is used without external switch in Fig 27. Pin 2 is the feedback terminal, used to regulate the output voltage as shown in Figs 27, 28, 29, and 30.
a first terminal;	The MOSFETs have a drain terminal.
a second terminal;	The MOSFETs have a source terminal.
a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;	The MOSFETs have a gate terminal that controls conduction from drain to source.
a drive circuit that provides said drive signal for a maximum time period of a cycle; and	This claim element lacks definiteness, because no oscillator or other cyclical process is included in the claim. However, the Unitrode publication includes an oscillator that has a maximum duty cycle, described at 9-348 and 9-349, whose signal is created by the flip-flop toggled by the sawtooth waveform tripping thresholds at 2.65V and 0.2V. For the UCC3801, -04, and -05 types there is a maximum duty cycle signal generated by the type-T flip-flop shown in Fig 1, and further described in the corresponding datasheets.
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.	The soft-start circuit is shown in block diagram form in Fig 1, and described in greater detail at 9-352.
10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.	The oscillator has a maximum duty cycle, described at 9-348 and 9-349, whose signal is created by the flip-flop toggled by the sawtooth waveform tripping thresholds at 2.65V and 0.2V. For the UCC3801, -04, and -05 types there is a maximum duty cycle signal generated by the type-T flip-flop shown in Fig 1, and further described in the corresponding datasheets.
14. The regulation circuit of claim 9 further comprising a frequency variation circuit that	N.A.

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provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.	
16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.	This claim lacks definiteness, because Claim 9 does not include an oscillator. However, Fig 27 shows the UCC3803 in a buck converter with monolithic switch, oscillator, drive circuit, and soft-start circuit.
18. The regulation circuit of claim 9 further comprising a rectifier comprising	See below.
a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectifier signal;	Off-line applications are described at 9-358, understood by one of skill to be transformerless rectified and filtered AC line input. Explicit circuitry to that effect is shown in Unitrode App Notes U-96A and U-100A, both referenced in U-133.
a power supply capacitor that receives said rectified signal;	See above. However, note that there is no antecedent "rectified signal," perhaps resolved by assuming that the penultimate word of the preceding claim element should have been "rectified."
a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and	This configuration is shown in Fig 31.
a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.	Shown in Fig 31.